# Example of a PSpice Comparator Macromodel

***Extra Material for use with the Book:***
***Pspice© Simulation of Power Electronics Circuits,***
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**Section 1.4.4 (***See Appendix E in the book)*

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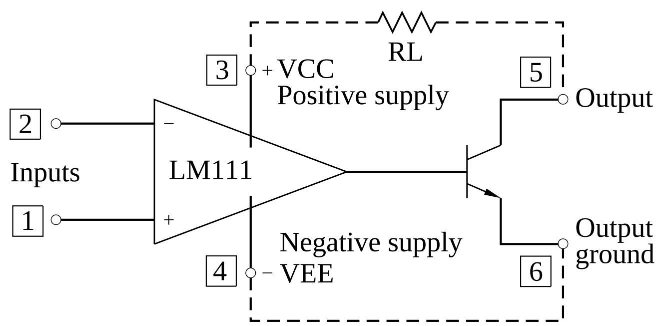
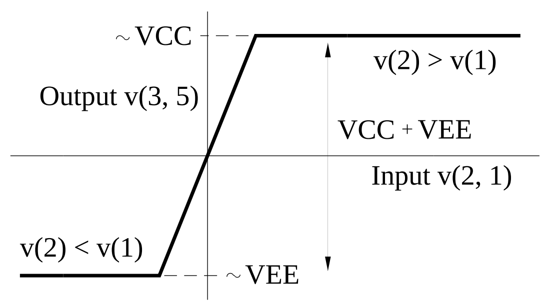
## 1.4.4 PSPICE COMPARATOR MACRO MODEL

The use of an analogue behavioural model (VCVS E) has proved to give near-ideal results of a comparator in Section 1.4.3. Job times were short and few nodes were needed. The comparator has a macromodel built into PSpice's library file EVAL.LIB. Inspect it; it models the comparator LM111, a silicon monolithic integrated circuit suitable for driving lamps, relays and solenoids. It is found in EVAL.LIB in a subcircuit with the name LM111. See Fig. 1.4.4.




(a)

**Fig. 1.4.4** The LM111 comparator.
(a) PSpice configuration,
(b) characteristics.




(b)

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* Refer PSpice to the appropriate library file.
. LIB        EVAL.LIB

* The next statement calls the comparator model into the circuit file.
Xcomparator    1   2   3   4   5   6   LM111;      X signifies a subcircuit.
*    |         |   |   |   |   |   |     |
*    |         |   |   |   |   |   |     Subcircuit name in library.
*    |         |   |   |   |   |   Output ground.
*    |         |   |   |   |   Node for output.
*    |         |   |   |   Node for negative supply, VEE.
*    |         |   |   Node for positive supply, VCC.
*    |         |   Node for inverting input connection (−).
*    |         Node for noninverting input connection (+).
* Device name in main circuit.
* The node numbers can be arbitrary.  The order of the comparator
* connections is important.
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These statements will be recognised in the example that follows.

There are several different ways to use the LM111 comparator. A common way is to treat the comparator as an open-collector output. The output-ground pin is connected to the system ground or VEE. The load is connected between the output pin and VCC. BJT turn-on occurs if the noninverting input voltage v(1) is less than the inverting input voltage v(2). Turn-on in accompanied by (VCC + VEE) appearing across the load resistor RL. Otherwise, the voltage across the load is virtually zero.

The load resistance value has to be set so that the load current does not exceed 50mA. Too high a value for $R_l$ results in a slow voltage rise-time as the output "floats" high.

## EXAMPLE W1.4.4

Repeat EXAMPLE 1.4.3 of the text using the PSpice comparator, model LM111. Use the load connection shown in Fig. 1.4.4 with a load value $R_l = 500\Omega$. Plot the traces of the input and output-voltage waveforms. Note the job time.

**Solution**

There are four steps to achieve a solution.

STEP 1

From Fig. EX1.4.3a we can draw the PSpice configuration using the subcircuit LM111 to represent the comparator. See Fig. 1.4.4.

STEP 2

From the PSpice configuration in Fig. 1.4.4 and the description of the comparator as a subcircuit above, we can write a circuit file W1_4_4.CIR. See next page.

STEP 3

The PSpice simulation is run with the circuit file W1_4_4.CIR. The results, input and output voltages as functions of time, are written in the file W1_4_4.DAT for the use of PROBE.

STEP 4

We can use PROBE to create traces of the sinusoidol input voltage v(2, 1) and the output voltage v(3, 5) as shown in Fig. W1.4.4 on the next page. As expected, if $v(2) > v(1)$ the output voltage v(3, 5) is 30V. Otherwise, the output voltage is zero. With this macro model LM111 the output-voltage rise-time is 8ms, but the fall-time is 30ms. These are slow responses. The job time was 9.62s, almost two seconds less that the job with the analogue behavioural model in EXAMPLE 1.4.3.

» » » » » W1_4_4.CIR » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » » »

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LM111 COMPARATOR FOR ZERO-CROSSING DETECTION
* To determine the input and output waveforms.

* SOURCES
VS      2   1   SIN(0  1V  1Hz);          Input voltage.
VCC     3   0   DC     15V;               Device positive source.
VEE     0   4   DC     15V;               Device negative source.

* CIRCUIT ELEMENT and DEVICE
RL      5   3   500 ohms;    Load resistance between collector and VCC.
Xcomparator     1  2  3  4  5  4  LM111;  Subcircuit call.

* Subcircuit for library file.
. LIB    EVAL.LIB

* ANALYSIS
. TRAN     3ms     1.6s
. PROBE    v(2, 1),   v(3, 5);    To view input and output voltages.
. END
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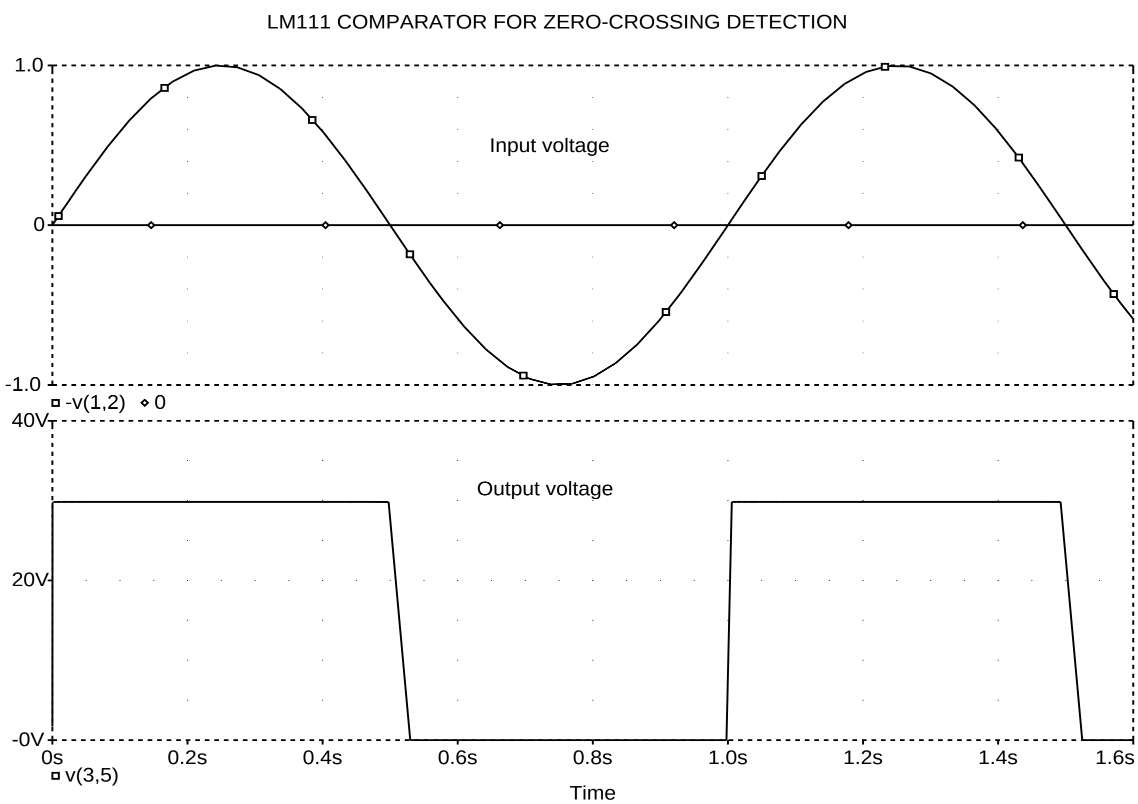


**Fig. W1.4.4**

END OF EXAMPLE W1.4.4

**Drill Exercise WD1.4.1**

Repeat Drill Exercise D1.4.5 (in the text) using the comparator LM11 from the file EVAL.LIB, but changing the load resistance to $R_l = 500\Omega$. Compare the results.

**Drill Exercise WD1.4.2**

Repeat Drill Exercise D1.4.6 using the comparator LM111 from the file EVAL.LIB and having a load resistance $R_l = 500\Omega$. Compare the results.

**Drill Exercise WD1.4.3**

Repeat Drill Exercise D1.4.7 using the comparator LM111 from the file EVAL.LIB, and having a load resistance $R_l = \Omega$. Compare the results.